What is claimed is:

1. A semiconductor circuit comprising:

an output circuit connected to a first power supplying terminal and a reference terminal for outputting an output signal, the output circuit having a plurality of first transistors serially connected between the first power supplying terminal and the reference terminal;

an input circuit connected to a second power supplying terminal and the reference terminal for receiving the output signal, the input circuit having a plurality of second transistors serially connected between the second power supplying terminal and the reference terminal, one of the second transistors having a gate for receiving the output signal; and

an input protection circuit connected to the output circuit and the input circuit;

wherein each of the first and second transistors has a gate, a source having a first low resistance region around a first contact formed thereon so that a first high resistance region is located between the gate and the first low resistance region, and a drain having a second low resistance region around a second contact formed thereon so that a second high resistance region is located between the gate and the second low resistance region.

2. A semiconductor circuit according to claim 1,

wherein the low resistance region is formed of a compound containing silicon and a metal.

3. A semiconductor circuit according to claim 2, wherein the low resistance region is a salicide layer region.

4. A semiconductor circuit according to claim 1, wherein the high resistance region is formed of a diffusion layer.

5. A semiconductor circuit according to claim 1, wherein the input circuit further has a plurality of third transistors each of which has a gate connected to one of the second transistors and a source and a drain both of which has an entire low resistance region.

6. A semiconductor circuit according to claim 5, wherein the entire low resistance region is formed of a compound containing silicon and a metal.

7. A semiconductor circuit according to claim 6, wherein the entire low resistance region is a salicide layer region.

8. A semiconductor circuit according to claim 1, wherein the first transistors have a PMOS transistor having a gate, a drain and a source connected to the first power supplying terminal, and an NMOS transistor having a gate connected to the gate of the PMOS transistor, a drain connected to the drain of the PMOS transistor and a source connected to the reference terminal.

9. A semiconductor circuit according to claim 1, wherein the first transistors include

a first PMOS transistor having a gate, a drain and a source connected to the first power supplying terminal,

a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, a source connected to the drain of the first PMOS transistor and a drain,

a first NMOS transistor having a gate connected to the gates of the PMOS transistors, a drain connected to the drain of the second PMOS transistor and a source, and

a second NMOS transistor having a gate connected to the gates of the PMOS transistors, a drain connected to the source of the first NMOS transistor and a source connected to the reference terminal.

10. A semiconductor circuit according to claim 1, wherein the first transistors include

a first PMOS transistor having a gate connected to the reference terminal, a drain and a source connected to the first power supplying terminal,

a second PMOS transistor having a gate, a source connected to the drain of the first PMOS transistor and a drain,

a first NMOS transistor having a gate connected to the gate of the second PMOS transistor, a drain connected to the drain of the second PMOS transistor and a source, and

a second NMOS transistor having a gate connected to

the first power supplying terminal, a drain connected to the source of the first NMOS transistor and a source connected to the reference terminal.

11. A semiconductor circuit according to claim 1, wherein the first transistors include

a first NMOS transistor having a gate connected to the first power supplying terminal, a source and a drain connected to the first power supplying terminal,

a first PMOS transistor having a gate, a source connected to the source of the first NMOS transistor and a drain,

a second NMOS transistor having a gate connected to the gate of the first PMOS transistor, a drain connected to the drain of the first PMOS transistor and a source, and

a second PMOS transistor having a gate connected to the reference terminal, a source connected to the source of the second NMOS transistor and a drain connected to the reference terminal.

12. A semiconductor circuit comprising:

a first circuit operating by an electrical power supplied from a first power supplying terminal and a reference terminal, the first circuit outputting an output signal and having a plurality of first transistors serially connected between the first power supplying terminal and the reference terminal;

a second circuit operating by an electrical power

supplied from a second power supplying terminal and the reference terminal, the second circuit receiving the output signal and having a plurality of second transistors serially connected between the second power supplying terminal and the reference terminal, one of the second transistors having a gate receiving the output signal; and

an input protection circuit connected to the first and second circuits;

wherein each of the first and second transistors has a gate, a source having a first low resistance region around a first contact formed thereon so that a first high resistance region is located between the gate and the first low resistance region, and a drain having a second low resistance region around a second contact formed thereon so that a second high resistance region is located between the gate and the second low resistance region.

13. A semiconductor circuit according to claim 12, wherein the low resistance region is formed of a compound containing silicon and a metal.

14. A semiconductor circuit according to claim 13, wherein the low resistance region is a salicide layer region.

15. A semiconductor circuit according to claim 12, wherein the second circuit further has a plurality of third transistors each of which has a gate connected to

one of the second transistors and a source and a drain both of which have an entire low resistance region.

16. A semiconductor circuit according to claim 15, wherein the entire low resistance region is a salicide layer region.

17. A semiconductor circuit comprising:

a first circuit receiving an electrical potential supplied from a first power supplying terminal and a reference terminal, the first circuit generating a signal and having a plurality of first transistors serially connected between the first power supplying terminal and the reference terminal;

a second circuit receiving an electrical potential supplied from a second power supplying terminal and the reference terminal, the second circuit receiving the signal output from the first circuit and having a plurality of second transistors serially connected between the second power supplying terminal and the reference terminal, one of the second transistors having a gate receiving the output signal; and

an input protection circuit connected to the first and second circuits;

wherein each of the first and second transistors has a gate, a source having a first low resistance region located around a plurality of first contacts formed thereon and a first high resistance region located between the gate and the first low resistance region, and

a drain having a second low resistance region located around a plurality of second contacts formed thereon and a second high resistance region located between the gate and the second low resistance region.

18. A semiconductor circuit according to claim 17, wherein the low resistance region is formed of a compound containing silicon and a metal.

19. A semiconductor circuit according to claim 17, wherein the low resistance region is a salicide layer region.

20. A semiconductor circuit according to claim 17, wherein the second circuit further has a plurality of third transistors each of which has a gate connected to one of the second transistors and a source and a drain both of which have an entire low resistance region.